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chapter 31

DADTA IV: A COMPUTER BASED VIDEO DISPLAY CONTROL AND DATA COLLECTION SYSTEM FOR BEHAVIORAL TESTING

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In the past five years the small, general purpose digital computer has become a common feature in many neurobiology laboratories, but to a considerable extent it has remained a tool of the electrophysiologist. Application of the minicomputer to the problems of the experimental analysis of behavior has been relatively limited and real-time computer systems for stimulus control and data collection are still somewhat uncommon.

The authors are deeply indebted to Jon Glick, who designed and constructed much of the hardware, and to R. Bruce Rule and James Bright, who are responsible for the extensive library of useful software available. We also wish to thank Dr. Robert Phelps for frequent and timely advice, Reese Cutler for aid in maintaining the hardware, and Dr. Carol Christensen for assisting with the preparation of the manuscript and figures. This work was supported in part by NIMH Grant MH 12970.

Precise, automated control of the contingencies which guide or produce behavior is almost universal in behavioral studies, as is some method for the unequivocal recording of behavioral effects of interest. The control systems employed are generally composed of hard-wired logic modules in combination with cumulative event counters or graphical output devices for the collection and recording of data. This approach is eminently satisfactory for the great variety of operant techniques characterized by a simple logical structure, and where the behaviors of interest are accurately reflected. However, in many discrimination paradigms the fine grain of behavior, such as reaction time, is of interest and the relevant data can only be obtained by detailed analysis on a trial by trial basis. The implementation of the necessary computational capabilities and output facilities with logic modules can become quite complex and it is often difficult to retain the desired degree of flexibility. These limitations and the use of increasingly complex discrimination paradigms provided the original impetus to seek more versatile alternatives to hard-wired logic systems and the rationale remains much the same today.

The computer based video display and control system described in this chapter is a descendent of a special purpose digital processor christened DADTA, for Discrimination Apparatus for Discrete Trial Analysis, designed and constructed some fifteen years ago in this laboratory (Pribram, et al., 1962) and resembles in many respects its immediate predecessor, DADTA III (see Pribram, 1969). The development of DADTA IV represents an attempt to take advantage of the then current (1970) display and minicomputer technologies to produce a general purpose system for the analysis of behavior. Although our primary applications relate to visual discrimination performance in non-human primates, the intent was to achieve sufficient generality and simplicity that DADTA IV would be useful in other laboratories and easily duplicated.

Moderate cost (about \$10,000 for a minimal configuration) was a prime design objective, but wherever possible and cost effective, commercially available system elements were employed. Particular emphasis was placed on developing a flexible method for stimulus presentation and minimizing the complexity of user constructed devices.

DESIGN CONSIDERATIONS

A variety of processors meeting the requirements of the DADTA IV were evaluated and the decision to select the PDP-8/e was based partially on considerations of our own experience with the PDP-8 family, compatibility with other computers in the laboratory, and our library of applications software. However, availability of peripherals, system software, and service facilities also figured heavily in the decision process. For similar reasons DECTape magnetic tape was chosen for mass storage of programs and data.

The selection of a general method for the presentation of visual stimuli presents many problems that are beyond the scope of this discussion, but some of the factors will be briefly outlined.

Probably the most common method of generating patterns for visual discrimination experiments involves the use of one or more individual display readouts. Typically these devices employ rear projection of a film mask onto a single-plane viewing surface and incorporate multiple bulbs permitting programmed selection of a small stimulus set, typically ten to twelve different patterns. If it is necessary to change the stimulus set the entire readout unit or the film mask must be changed -- at best a time consuming process that cannot, of course, be done under program control. Another serious drawback is that the readout is located at a fixed position in space. If a paradigm calls for the presentation of stimuli in a variety of spatial positions, it is necessary to employ multiple readouts. This was the approach taken with DADTA III which employed a 4x4 square array of 12 symbol projection units for display purposes (Pribram, 1969). The multiple readout method requires a fair amount of decoding and power driving hardware, cabling and maintenance.

Sequential or random access 35 mm slide projectors represent another alternative method for programmed display of complex spatial patterns of arbitrary nature, but the unreliability and slowness of the electromechanical components, the need to photographically prepare all stimulus configurations, and the inability to easily create dynamic patterns limit the usefulness of the technique.

It is clear that the ideal device for this application would offer a large surface area on which complex spatial patterns could be generated with good, programmed control over visually important parameters such as luminance, contrast, rise time, and chromaticity. This ideal can be only distantly approached at the present, but a number of CRT and plasma graphics devices exhibit some of these desirable characteristics.

Large screen electrostatically deflected CRTs directly refreshed by the CPU offer good spatial resolution, but are expensive and the generation of even moderately complex patterns places excessive demands on the processor to the point where display flicker becomes a limiting factor. Most self refreshed CRT displays incorporating internal memories are character and text oriented and do not offer the desired degree of flexibility.*

Large screen storage tube displays (e.g., the Tektronix 611) offer economy, freedom from refresh requirements and good graphics capabilities but the stored image has poor luminance and contrast qualities and control over these important parameters is limited.

The use of a scan conversion technique to generate a television video signal from the information written on a special storage CRT was selected for DADTA IV, thus retaining several of the advantages offered by the storage CRT while gaining the desirable contrast and luminance characteristics of a television monitor.

The low cost of the actual display device (\$100 - \$500 for a typical video monitor) is a distinct advantage because it is economically feasible to locate parallel display monitors in a number of locations for monitoring of the stimulus display during experiments or program development. Additionally the critical and expensive display hardware can be kept out of the harsh environment of the animal testing chamber. Finally the ability to modify the computer originated display by mixing the scan converter output with external video sources (eg. a

* Extremely fast, internally refreshed high resolution displays have been built, but the expense is prohibitive for most applications. Continued advances in memory technology will hopefully bring the cost to a reasonable level in the not too distant future.

spatial white noise signal or a masking pattern) proves useful in some applications.

It is recognized that the performance of television raster scan displays is only marginally suitable for many visual experiments because of the limited spatial and temporal resolution. The scan converter employed in DADTA IV can resolve approximately 100 lines vertical and 125 lines horizontal and the "frame" rate is 30 per second. For virtually all behavioral studies and for some types of electrophysiological stimulation these characteristics are acceptable.

SYSTEM ORGANIZATION

Physically the DADTA IV system is constructed in two enclosures.

1) The computer and peripheral rack contains the PDP-8/e processor and internal options, the Tektronix Type 4501 Scan Converter unit, DECTape transports, power supplies and A/D converter input panel.

2) The testing chamber consists of a sound attenuated enclosure for the subject, subject response panels, the video display monitor and reinforcement dispensers. A small interface box on the rear of the chamber contains the connectors that receive cables from the computer rack, the drivers and power supply to control and provide the current for operating testing chamber devices (e.g., chamber lighting and reinforcement dispenser) and the signal conditioning buffers for the subject response switches.

In the usual configuration for discrimination testing, the face of the CRT is overlaid with a 3x3 matrix of transparent plastic disks, each mechanically coupled to a microswitch. Discriminanda are displayed in positions behind the disks and depression of a panel constitutes the subject's response. In effect the video display is being used to simulate a set of nine individual display devices. The overlay is easily removed for paradigms not requiring a response spatially associated with the stimulus or the number and geometry of response regions can be quickly altered by substituting a different switch panel (see figure 1).

The processor enclosure and testing chamber are linked by two flat ribbon cables and a single coaxial

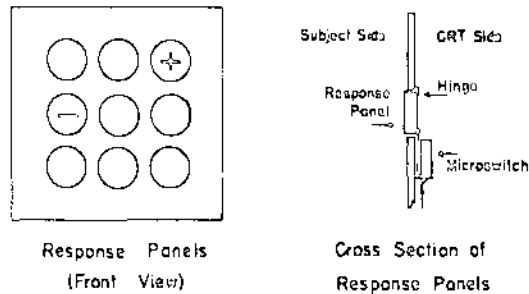


Figure 1. Configuration for discrimination testing.

cable carrying the video signal. The cables are limited to a maximum of ten meters in length.

Figure 2 indicates the overall organization of the DADTA IV system presently in use. Devices not essential to the operation of a minimal configuration are indicated with a star. Processor options, I/O channels, the real time clock and controllers for all the peripherals except the scan converter are mounted on the PDP-8/e processor which is equipped with a total of 12k words of memory. Although most applications can be written to run in 4k, the very useful DEC operating system, OS/8, requires a minimum 12k configuration (or 8k and a read-only-memory) when operated with the TD8-E DECTape system.

Operator interaction with the DADTA IV is via a teletype which also serves as a hard copy output device. In the minimal system, not including magnetic tape storage, the paper tape reader is used for program loading. The TD8-E DECTape control and TU56 dual tape transports provide the medium for program and mass data storage. Generally DADTA IV is operated under OS/8 or X/SYS software operating systems which provide convenient tape library facilities. The TD8-E is a rather primitive non-interrupt, non-data break controller with the saving grace that it is an order of magnitude less expensive than the more elegant TCO-8 controller. Since the primary role of the magnetic tape in the DADTA IV is program storage, the slow, CPU intensive data transfers are not a serious problem.

The time base for applications programs is provided by the DK8-E real time clock which is programmed to interrupt the processor at 1 msec. intervals, at which time a software clock is updated.

The major communication channel between the processor and the external world is the DR8-EA static I/O

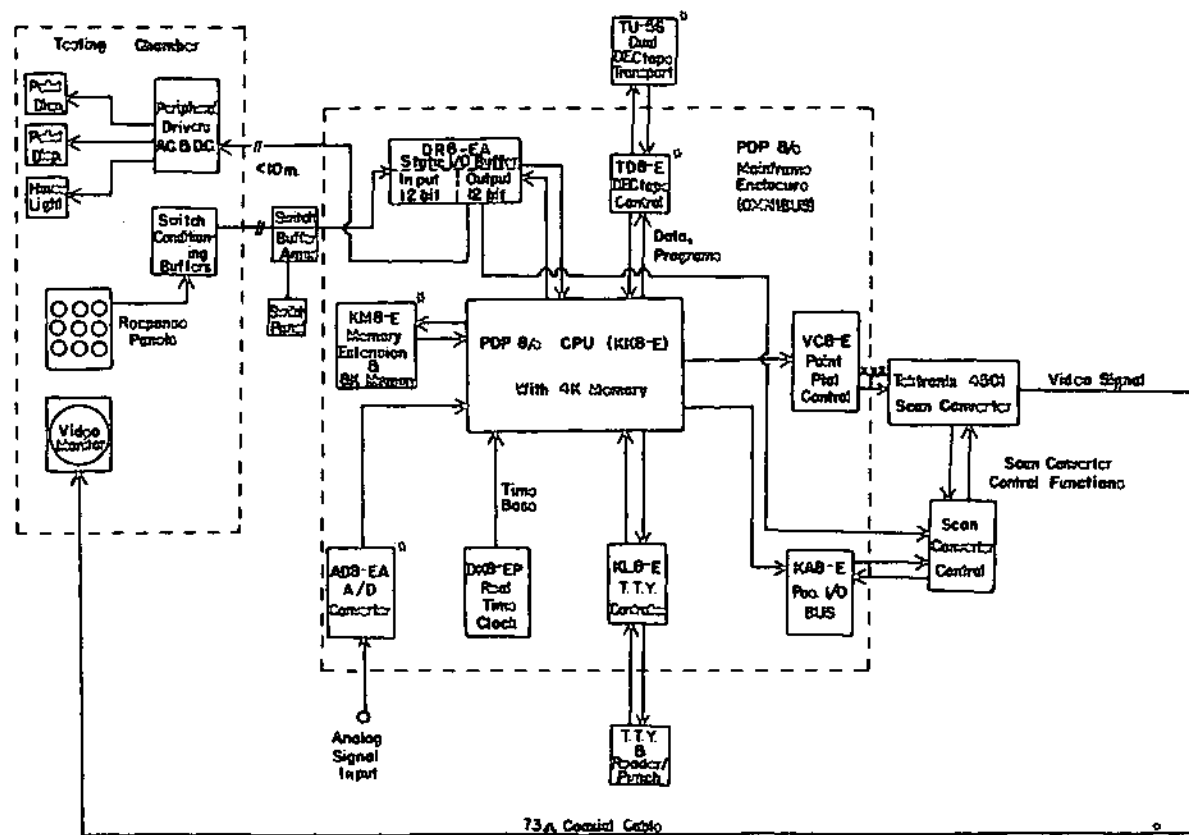


Figure 2. Block diagram of DADTA IV system presently in use.

buffer. The output portion of the buffer is a 12-bit register that can be loaded, cleared or read by the processor providing simple switching control of low speed peripherals. Eight bits are allocated for control of testing chamber functions and four are reserved for selection of display options. The 12-bit input buffer is identical to the output buffer except that the register bits are normally set by external events and only the input buffer is connected to the interrupt line. All subject responses are input via the DR8-EA. The positive I/O bus interface is included on the Omnibus to permit the implementation of input-output transfer (IOT) instructions for peripheral controllers constructed with Digital Equipment Corporation (DEC) logic modules. It was felt that the use of the external positive I/O bus rather than direct interfacing with the Omnibus would reduce the complexity of the scan converter control and facilitate system expansion by other users.

TESTING CHAMBER INTERFACE

The testing chamber interface is constructed from DEC K-series modules mounted in a K724 interface shell and communicates with the static I/O buffer via a flat ribbon cable (maximum length of 10 meters). The K-series logic exhibits excellent noise immunity.

1) Output Section (shown in figure 3): Bits 04 to 09 of the DR8-EA, after inversion, drive the gated inputs of the peripheral device current drivers. Bits 04 to 07 control isolated A.C. switches (rated at 500 V.A.) whereas bits 08 and 09 control D.C. switches (1A. at 55V.). Bits 10 and 11 are one-shot coupled to the D.C. drivers for triggering pulse operated devices. In the usual discrimination configuration of DADTA IV the pulsed D.C. outputs operate reinforcement dispensers, one A.C. driver controls testing chamber illumination and the remaining switches are uncommitted and available for special requirements.

2) Input Section (shown in figure 4): Twelve slowed K123 buffer gates provide switch conditioning and line drive to transmit switch closure information to the static input buffer. The lines are also buffered at the receiving end where a parallel set of switch inputs is available. As shown, nine of the testing chamber inputs are committed to the subject response panels. The

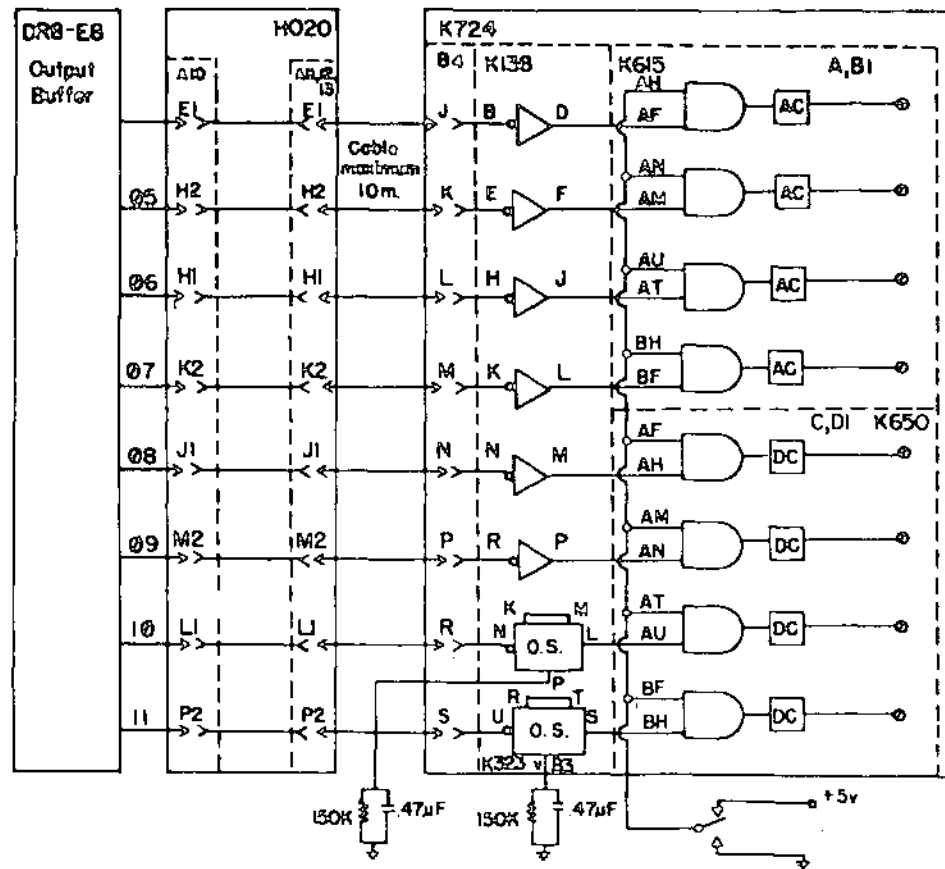


Figure 3. Output buffer and drivers for peripheral equipment.

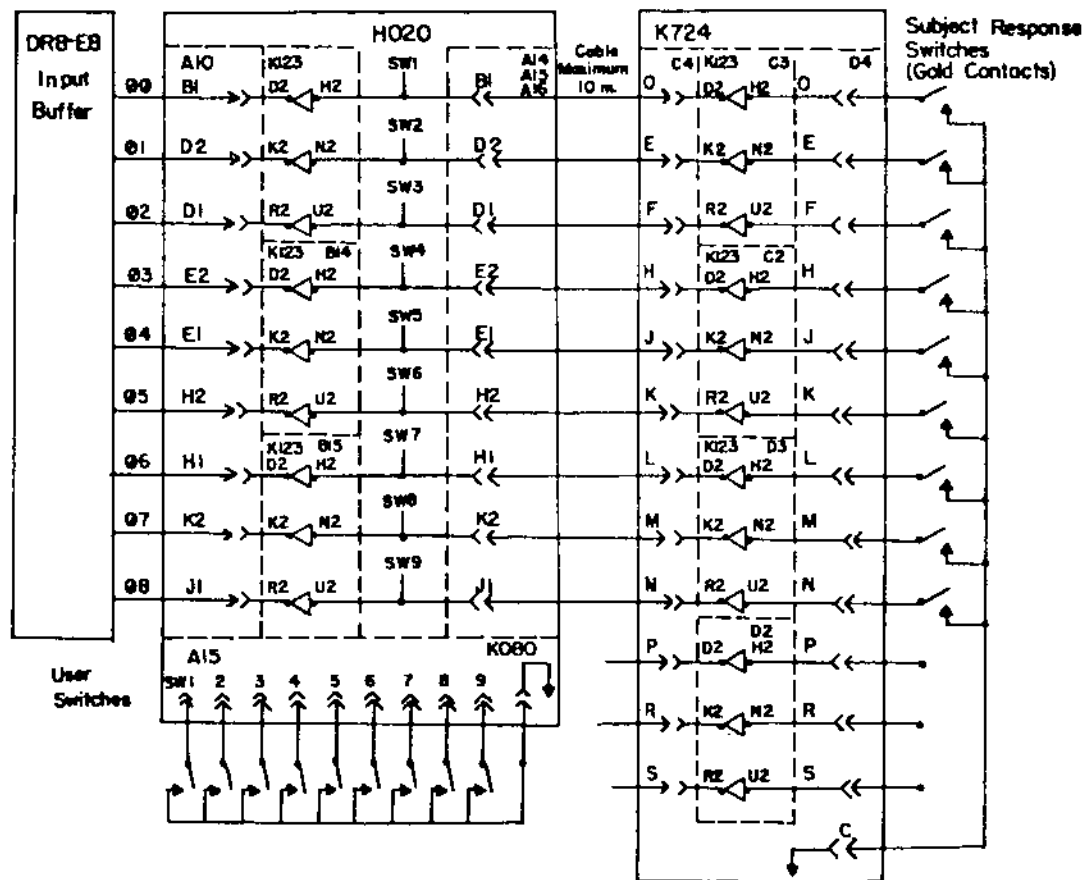


Figure 4. Output drivers and buffers for user switches and subject response switches.

parallel switch set at the computer end is particularly useful during program checkout if the testing chamber is located remotely.

DISPLAY HARDWARE

The Tektronix Type 4501 scan converter serves both as an image storage medium for non-dynamic displays and as an interface element between the processor and the video display monitors. Write-in is accomplished by supplying x and y deflection information from the VR8-E point plot control (high speed dual channel D/A converter) along with the appropriate intensity modulation (z axis). Although the resolution of the VR8-E is 10 bits on both the x and y axes the scan converter coordinate system has a 4x3 aspect ratio corresponding to the dimensional characteristics of a conventional television frame. The storage principles of the scan converter are similar to those of the conventional storage oscilloscope but the CRT storage target is constructed in a manner that allows read-out of the stored information by scanning the target with a "read beam" in a systematic manner. The Type 4501 scans in a pattern corresponding to a television raster and develops the necessary synchronization and blanking pulses to produce an E.I.A. standard 525 line composite video signal. A signal beam is used for both reading and writing and it must be time shared in situations where it is necessary to update the display without interrupting the video output or if displays are being generated with the scan converter in the "non-store" mode. The beam time sharing dictates certain timing requirements for data transfer from the CPU and these will be discussed when the scan converter control hardware is described.

There are several operational modes for the 4501 which in DADTA IV are selectable either manually or by program instructions. The options are:

- 1) Dark/light background: The written area of the CRT may be selected to appear as white on a black level background or black on a white level.
- 2) Read only: In "read only" mode the storage target is scanned and a video signal is produced from the stored information, but no new information can be written.

3) Write only: In "write only" mode, read raster scanning is disabled and the video output is held at background level. New information may be written on the target and stored for subsequent readout.

4) Store/non-store: In store mode information written on the tube face is retained for periods of up to 15 minutes. In non-store mode information is not retained beyond the normal target persistence time.

SCAN CONVERTER CONTROL

Option mode selection is controlled by bits 00 to 03 of the DR8·EA static output buffer (figure 5). Setting a bit in the buffer enables the corresponding buffer gate which activates the 4501 control input line. The static buffer bit allocations are summarized in Table 1. If neither "read only" nor "write only" is selected, the mode of operation will be "read and write".

Stored information is removed from the display by selecting the scan converter erase function. Selective data erasure is not possible. The entire screen must be erased, modified and rewritten to delete a portion of the stored image. The erase function is implemented as an I.O.T. instruction via the KA8·E positive I/O bus and appropriate device selector. A complete 4501 erase cycle requires 174 msec., during which time the video output is gated off. However, if an erase instruction is issued while read scanning is in progress, a transient flash of light and loss of monitor synchronization may occur. This problem can be avoided by only initiating erase cycles during the vertical blanking interval. A negative going vertical drive level with the leading edge coincident with the start of vertical blanking is available and is used to provide programmed detection of the start of the vertical interval. The "erase cycle in progress" level from the scan converter is OR'd with the level shifted and inverted vertical drive to furnish the I.O.P. gating signal. The resulting I.O.T. instruction, "skip on vertical drive on or erase cycle in progress" minimizes hardware requirements while providing all information necessary for proper erase timing. It would, of course, be straightforward to handle all erase cycle timing directly with hardware.

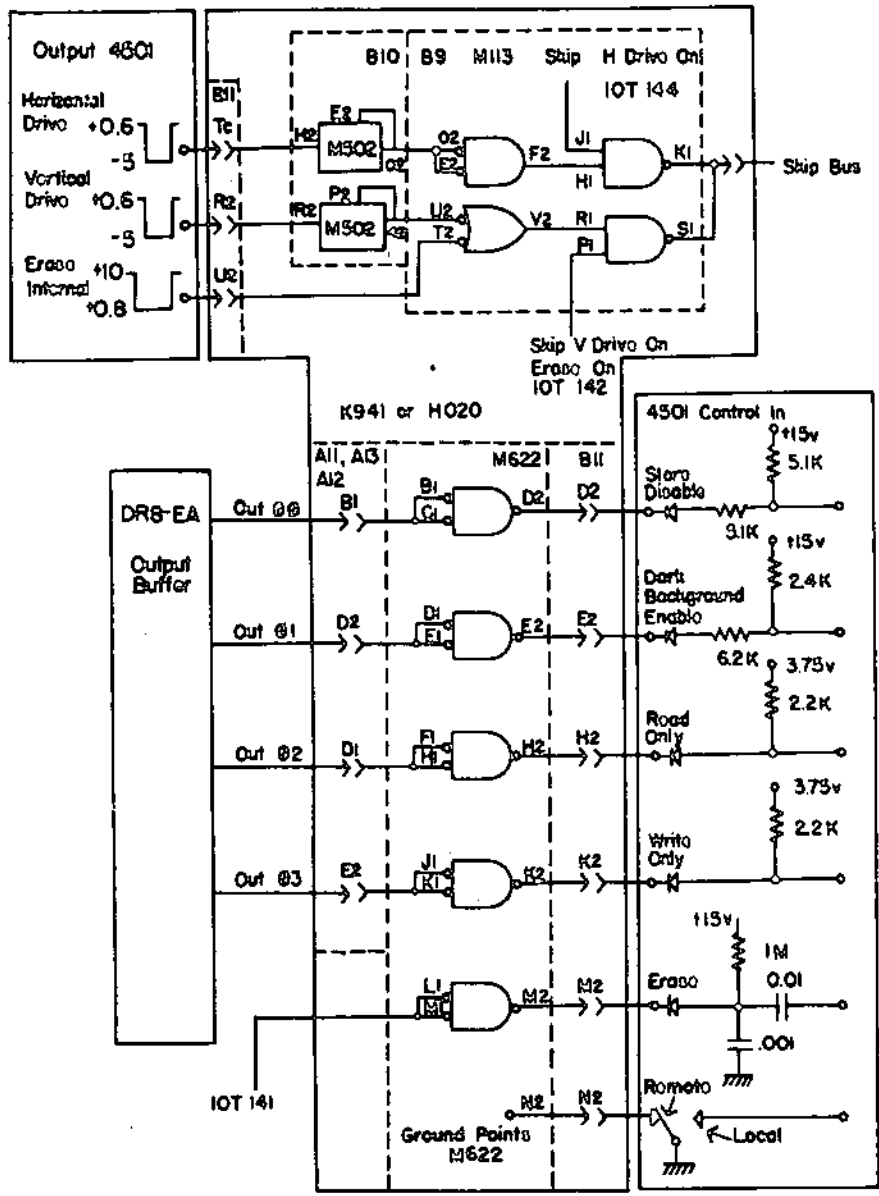


Figure 5. Control for Tektronix 4501 Scan Converter.

Table 1. Scan Converter Control Options.

<u>Option</u>	<u>Output Buffer Bit</u>
store/non-store	00
dark/light background	01
read only*	02
write only*	03

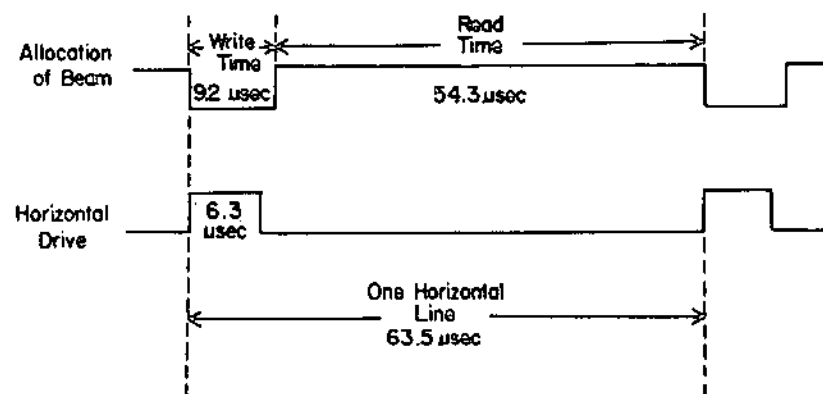
Scan Converter Control I.O.T. Instructions

<u>I.O.T.</u>	<u>Instruction</u>
6141	Erase display
6142	Skip if vertical drive on or erase cycle in progress
6144	Skip if horizontal drive on

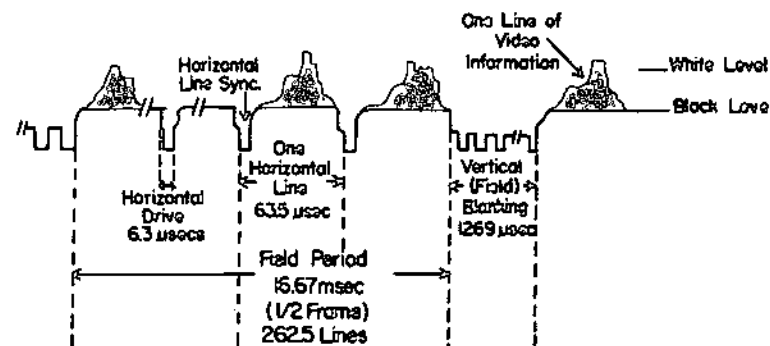
* If neither "read only" nor "write only" is asserted, the default condition is "read and write".

The scan converter control includes a flag indicating the start of the interval between successive horizontal scan lines. The horizontal drive level from the 4501, after level shifting and buffering, gates I.O.P. 4 to give a "skip on horizontal drive on" I.O.T. instruction. This instruction is used for proper synchronization of data transfer from the VC8-E point plot control when the scan converter is operated in the "read and write" mode. In this mode, read scanning and video output are maintained continuously, but the beam is available for writing during the 9.2 usec between the end of each horizontal line and the beginning of the next (see figures 6a and b). Generally only one point can be written in each line interval since the scan converter requires 8 usec (maximum) to write a point in "store" mode. This limits the maximum writing rate to 15,725 points per second. The programmer must be somewhat careful to pre-load the D/A converter registers to ensure

that sufficient time will be available to deflect the write beam and intensify the point within the write time slice. The "read and write" mode can be used in non-store mode for generation of dynamic displays as the target persistence is sufficient to maintain a point until the next line scan. In the current controller, the scan converter flags are not connected to the interrupt line. However, in some applications where the demands on the CPU are heavy it might be desirable to do so.



6a



6b

Figure 6. Timing diagrams for scan converter. (a) Scan converter beam share timing in "Read and Write" mode. (b) Video signal (simplified).

SYSTEM PERFORMANCE

DADTA IV has been operational for approximately three years (more than a dozen neurobehavioral experiments have been run and completed) and has proven flexible and reliable in an environment where a variety of experiments with unique stimulus requirements are in progress simultaneously. The scan conversion technique produces moderately complex displays of good quality. Reliability of the entire system has been excellent and there have been no significant hardware difficulties.

A library of assembly-level subroutines including programs for certain display functions, time-keeping and response processing has been developed and these are integrated with control programs written in a real-time modified version of FORTRAN II. The use of compiler level coding greatly simplifies the task of handling computation, report generation, tape I/O, and operator interactions. The display software allows specification of stimuli in a variety of formats depending on the degree of flexibility required for a particular application. In a simple case, for example, only a panel position, a size parameter and a character from the standard set might be necessary to specify a stimulus, whereas a more complex display might require furnishing a set of stimulus descriptors for use by the more general graphics routines.

SYSTEM EXPANSION

A shortcoming of DADTA IV in its present form is that the processor is dedicated to the operation of a single testing station at any one time. Expansion of the system to handle multiple stations simultaneously is not difficult from either a hardware or software point of view, but requires the addition of a scan converter, scan converter control, and static I/O buffer for each additional independent display. This represents a hardware cost in excess of \$3000. If more than a few independent stations are contemplated, it becomes economical to use a single time shared scan converter for production of video signals and a multiple channel video disk recorder for refreshing the individual monitors. In multiple channel systems of either type the generation of

multicolor displays becomes feasible by allocating two or more channels to a single color monitor.*

FINAL COMMENTS

DADTA IV is primarily intended for behavioral testing applications, but the display system has been used for stimulus presentation in several electrophysiological investigations. It should be mentioned that some preliminary data from this laboratory suggest that there may be some problems associated with the use of television displays in single unit studies. Although the displayed images are well defined and flicker free to the human observer at usual intensity levels, the emitted light contains a large modulation component at the 60 Hz. scanning rate (i. e., the television field rate). Over small vertical screen distances the modulation components are nominally in phase and it appears that many visual system neurons are driven at the scanning rate when the animal is exposed to a bright spot stimulus within the unit's receptive field ** (Phelps, personal communication). Even with a modified scan converter and monitor operating at a 120 Hz scan rate, some visual units continue to respond to the scanning modulation although direct following does not occur. Regardless of whether this phenomenon produces alteration of normal visual information processing, the introduction of unintended noise within the bandpass of the system under study is definitely undesirable. Additionally there is some tentative evidence that under certain conditions intensity modulation of a visual stimulus at frequencies above the flicker fusion point may affect visual discrimination performance in the monkey (Christensen, 1973).

This type of problem is not unique to DADTA IV; all systems for stimulus presentation are less than ideal in

*The use of a color monitor in a single channel system will provide the capability to vary the chromaticity of the entire display. A very limited form of multicolor display could be obtained with some additional hardware.

**Lateral Geniculate and Area 17 of the unanesthetized cat.

TTL logic directly on the quad board, by a factor of 5 or 10.

DRAKE: That's certainly true, although it was less true at the time. We hoped this would appeal to psychologists who were used to working with logic modules but had no experience with computers.

MCINTYRE: The trick is to tell them the little ICs are miniature logic modules.

CLARKE: If you were putting this system together today, would you have used a 4501?

DRAKE: Tektronix doesn't make them anymore.

REFERENCES

1. Christensen, C. A. The Effects of Inferotemporal and Fovial Prestriate Lesions on Discrimination Performance in the Monkey. Unpublished doctoral dissertation. Stanford University, (1973).
2. Pribram, K. H., Gardner, K. W., Pressman, G. L., and Bagshaw, M. H. An automated discrimination apparatus for discrete trial analysis (DADTA). Psychol. Rev. 11:247-250 (1962).
3. Pribram K. H. DADTA III: An on-line computerized system for the experimental analysis of behavior. Percep. and Motor Skills 29:599-608 (1969).

For detailed information on Digital Equipment Corp. devices and systems the reader is referred to the following publications available from Digital Equipment Corp., Maynard Mass:

Small Computer Handbook. 1972
Control Handbook. 1971
Logic Handbook. 1972
Logic System Design Handbook. 1972

For detailed information on the Tektronix Type 4501 Scan Converter refer to:

Tektronix Type 4501 Scan Converter Unit Instruction Manual 1969. Available from Tektronix, Inc., Beaverton, Oregon.

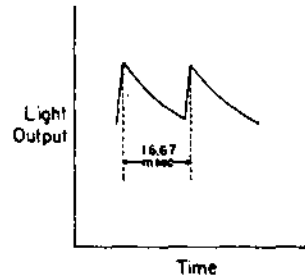


Figure 7. Modulation of light output from television screen.

some respects. Display and memory technologies are developing at a rapid rate and it is likely that the near future will bring a variety of low cost, self refreshed graphics displays potentially suitable for stimulus presentation in vision research. However, it should always be kept in mind that subtle differences between displays may exist that can influence experimental results in unpredictable ways. Stimuli generated by different methods may be perceptually equivalent or similar to the adult human observer, but this does not imply that they are equivalent to an animal or immature subject, particularly when we are dealing with a damaged or modified central nervous system. Furthermore, stimuli that are indistinguishable to the subject may not produce identical electrophysiological responses at all points in the sensory system. These obvious principles are often given too little consideration in the design of stimulus generation equipment for behavioral and even electrophysiological studies.

DISCUSSION

D.O. WALTER: Has this been exported?

DRAKE: In a few cases.

MCINTYRE: The decision about the I/O bus structure is a little odd. The cable costs and module costs could make your individual interfaces awfully expensive in comparison to the quad board or the alternative of using

APPENDIX I

MINIMAL DADTA IV SYSTEM

I. Computer Enclosure

D.E.C. PDP-8/e Processor with 4k words of memory
D.E.C. ASR 33 Teletype with paper tape punch/reader
D.E.C. KL8-E T.T.Y. Controller
D.E.C. DR8-EA 12-bit buffered I/O
D.E.C. VC8-E Display (point plot) Control
D.E.C. KA8-E Positive I/O Bus
Scan Converter Control (modules available from
D.E.C.)*

II. Testing Chamber

Television Monitor
Input Response Interface and Peripheral Output
Drivers (modules available from D.E.C.)*
5v. Power Supply for above
Davis PD 109A pellet dispensers

EXTENDED DADTA IV SYSTEM

In addition to the minimal system, the following are
suggested:

8k memory and extended memory control
D.E.C. DE8-E Extended Arithmetic Option
D.E.C. TD8/e DECTape Controller
D.E.C. TU-56 Dual DECTape Transports
D.E.C. AD8-EA A/D Converter
D.E.C. DK8-EP Real Time Clock

* Not commercially available